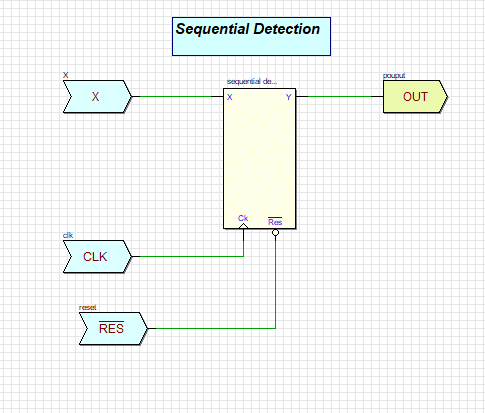
Sequential Detection



The following is a VHDL listing and simulation of a 0 1 1 0 sequence detectors. This listing includes the VHDL code and a suggested input vector file. In addition to giving the user more exposure to VHDL and sequential machines, this routine demonstrates the use of an input vector file for driving the simulation.

